Family 15h Models 00h-0Fh AMD FX™-Series Processor Product Data Sheet

Publication # **49686**
Revision: **3.00**
Issue Date: **October 2011**

Revision History

Date	Revision	Description
October 2011	3.00	Initial Public Release.

1 Features

The following is a list of features and capabilities of the Family 15h Models 00h-0Fh AMD FX™-Series processor.

- **Compatible with Existing 32-Bit and 64-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, SSE4a, SSE4.1, SSE4.2, SSSE3, ABM, AVX, AES, XSAVE/XRSTOR, PCLMULQDQ, FMA4, XOP, MMX™, and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip
  - Light Weight Process (LWP) support
- **AMD64 Technology**
  - AMD64 technology instruction-set extensions
  - 64-bit integer registers, 48-bit addresses
  - Sixteen 64-bit integer registers
  - Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers
- **Family 15h Architecture**
  - FPU shared between two cores
  - Support for up to 8 cores per node
- **Machine-Check Architecture**
  - Includes hardware scrubbing of L3 ECC-protected arrays
- **Cache Structures**
  - **16-Kbyte 4-Way Associative, Write-through ECC-Protected L1 Data Cache per Core**
    - Two 64-bit operations per cycle, 3-cycle latency
  - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache Shared between Two Cores**
    - With advanced branch prediction
  - **1024-Kbyte 16-Way Associative ECC-Protected L2 Cache Shared between Two Cores**
    - Exclusive cache architecture storage in addition to L1 caches
  - **8192-Kbyte (8-Mbyte) Maximum 64-way Associative Cache Shared between All Cores on a Node**
    - Shared cache architecture storage in addition to exclusive L1 and L2 caches
- **Flexible Floating-Point Unit**
  - 256-bit shared or two dedicated 128-bit floating-point units (FPU)
  - Shared between two cores
- **Managemement and Virtualization Features**
  - Advanced Platform Management Link (APML)
    - SMBus v2.0-compatible interface
    - Remote-Management Interface (SB-RMI)
  - AMD Virtualization™ technology (AMD-V™)
    - SVM pause count capability
    - SVM disable and lock
    - Rapid virtualization indexing (nested paging)
    - Improved world-switch speed

- **Power Management**
  - Multiple low-power states
  - Advanced Power Management
  - AMD Turbo CORE technology 2.0 with per core power gating
  - System Management Mode (SMM)
  - Hardware Thermal Control (HTC)
  - ACPI-compliant, including support for processor performance states
  - Supported power states: C0, C1, C1E, C6, CC6, S0, S3, S4, and S5
- **Electrical Interfaces**
  - DDR3 SDRAM: Compliant with JEDEC DDR3 1.5-V SDRAM specifications
  - Refer to the *AMD Family 15h Models 00-0Fh Processor Electrical Data Sheet*, order# 47079, for electrical details of AMD Family 15h processors.
- **HyperTransport™ Technology**
  - HyperTransport™ 3 technology supported
  - Maximum one (1) link on AM3r2 package, 16-bits in each direction, supporting up to 5200 MT/s (10.4 GB/s) in each direction in HyperTransport Generation 3.0 mode
- **Integrated Memory Controller**
  - AMD Memory Controller PowerCap
  - Low-latency, high-bandwidth
  - DRAM Prefetcher:
    - Adaptive prefetching support
    - 32-entry DRAM prefetch table
    - Differentiate between core prefetch requests and core demand requests
  - ECC checking with double-bit detect and single-bit correct
  - 144-bit DDR3 SDRAM controller operating at frequencies up to 1866 MT/s (933 MHz)
  - Package AM3r2
    - Supports up to four (4) unbuffered DIMMs
- **Available Packages**
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
  - Package AM3r2
    - Refer to the *AM3r2 Processor Functional Data Sheet*, order# 47707, for functional and mechanical details of the AM3r2 package processor.
    - 940-pin lidded micro PGA package
    - 1.27-mm pin pitch
    - 31-row x 31-col pin array
    - C4 die attach

2 Compatible Socket Infrastructures

Refer to the AMD *Infrastructure Roadmap*, order# 41842, for information on platform-feature implications of package and socket-infrastructure combinations. Family 15h Models 00h-0Fh AMD FX™-Series processors support the following socket infrastructures:

- **AM3r2 Socket Infrastructure**
  - Compatible with AM3 and AM3r2 package processors
  - Refer to the *AM3r2 Processor Functional Data Sheet*, order# 47707, for functional and mechanical details of the AM3r2 socket infrastructure.